105. The method according to claim 104, wherein said initially setting step comprises a step of setting control data through at least one input line.

106. The method according to claim 103, wherein said actual written states of said memory cells are simultaneously determined.

107. The method according to claim 103, wherein a selectively modifying step comprises simultaneously modifying control data stored in said plurality of programming circuits in accordance with said predetermined logical relationship.

108. The method according to claim 103, further comprising selectively changing voltages applied to said memory cells according to said stored control data.

109. The method according to claim 108, further comprising selectively and simultaneously changing said voltages of said bit lines applied to said memory cells.

110. The a method according to claim 103, wherein said selectively modifying step is continued until each memory cell is sufficiently written.

111. The method according to claim 103, wherein said modifying and applying step is repeated during a limited number of cycles.--

REMARKS

The claims added by this Second Voluntary Amendment were copied from patent no. 5,831,903 of Ohuchi et al., granted on November 3, 1998. These newly added claims are exact copies of claims 1-12 of the Ohuchi patent. They are being added to this application since they pertain to the same subject matter as currently being claimed. The '903 Ohuchi et al. patent from which they have been copied is a continuation of patent no. 5,657,270 of Ohuchi et al. from which claims were earlier copied into the present application.

A prompt examination and allowance of the present application is solicited.

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Respectfully submitted,

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